THE COMMISSIONER OF PATENTS AND TRADEMARKS Docket No. **TS98-518**
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the Patent Application of:

Inventor: **TZE-LIANG YING, JAMES WU, YU-HUA LEE AND WEN-CHUAN CHIANG**

For: **A KEY-HOLE FREE PROCESS FOR HIGH ASPECT RATIO GAP FILLING WITH REENTRANT SPACER**

Enclosed are:

[X] 3 sheets of drawing(s) - formal.

[X] An assignment of the invention to **Taiwan Semiconductor Manufacturing Company**

[ ] An associate power of attorney

The filing fee has been calculated as shown below:

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FOR:	NO. FILED	NO. EXTRA	RATE	FEE
BASIC FEE				$ 760.
TOTAL CLAIMS	**26** -20=	**6**	x 18 =	**$ 108.**
INDEP CLAIMS	**2** -3=	**0**	x 78 =	**$ 0.**
MULTIPLE DEPENDENT CLAIM PRESENTED			+ 260 =	
			SUB TOTAL	**$ 868.**
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Respectfully submitted,

STEPHEN B. ACKERMAN, REG. NO. 37,761

TS98-518

A KEY-HOLE FREE PROCESS FOR HIGH ASPECT RATIO GAP FILLING WITH REENTRANT SPACER

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the field of semiconductor manufacturing, and more specifically to a method to completely and satisfactorily fill high aspect ratio gaps.

(2) Description of Prior Art

The conventional method of forming conducting lines and connecting vias within the construct of a semiconductor device is to deposit a layer of conducting material, such as aluminum, on the surface of a semiconductor using for instance a sputtering technique. Over this layer of conducting material is deposited a layer of photoresist, this photoresist is patterned and etched such that the conducting material that is to stay in place (to form the conducting lines or vias) is covered or protected by the photoresist. The unwanted conducting material is then removed, typically using anisotropic plasma etch. The openings created by the removal of the conducting material are filled with a dielectric

material such as an oxide. The surface of the combined patterns of conductive material and dielectric can further be planarized by using a Chemical Mechanical Polishing (CMP) process that completes the creation of conducting lines or vias.

The formation of air gaps between conducting lines of high speed Integrated Circuits (IC's) is typically a combination of the deposition of a metal layer, selective etching of the metal layer to form the desired line patterns, the deposition of a porous dielectric layer or a disposable liquid layer which is then selectively removed to form the desired air-gaps.

By combining bias sputtering deposition techniques with plasma-enhanced deposition, a high deposition rate has been established for CVD oxide. The deposited CVD oxide is free from particles from chamber walls and from metallic contamination and can furthermore produce films of low stress. Needed to accomplish this deposition however is a source of high density, low-energy ions. High-density plasma sources provide the capability to combine CVD SiO_2 and bias sputtering for high quality Intra-Layer Dielectric (ILD) at a low temperature.

Recent requirements for the creation of holes within deep layers of either conducting or other materials have resulted in creating openings that have aspect ratios in excess of 3. It is beyond the capability of the existing techniques to fill gaps of this aspect ratio with High Density Plasma-oxide (HDP-oxide). This lack of adequate filling of gaps also occurs for holes that have a reentrant spacer profile. A reentrant spacer profile is a profile where the walls of the openings are not vertical but are sloped, this sloping of the walls makes complete penetration of the HPD-oxide into the hole difficult and, under certain conditions, incomplete.

As a consequence of incomplete deposition of HDP-oxide into high aspect ratio holes, keyholes or deposition irregularities will be formed. These keyholes or deposition irregularities are characterized by non-homogeneous deposition that form in the deposited HDP-oxide.

Fig. 1 shows Prior Art deposition of HDP-oxide 12 over a pattern 14 of polysilicon. The pattern 14 can be deposited on the surface of a semiconductor substrate 10 or on any other surface within the formation of a semiconductor device. The resulting keyhole 16 appears within the hole 13 and is approximately centered within the hole. The keyhole is formed

due to incomplete flow of the deposited HDP-oxide resulting in molecular tension and lack of uniform distribution of the deposited HDP-oxide.

Fig. 2 shows the same Prior Art phenomenon in the formation of the keyhole 16, in this example spacers 18 (for the SAC process) with a reentrant profile have been added to the polysilicon pattern 14. In the example shown in Fig. 2, the formation of the keyhole 16 can be more severe since the reason for the formation of the keyhole is further emphasized by the profile of the spacers 18. This profile shields portions of the holes between the poly pattern 14 from the source of the HDP-oxide deposition, this shielding further amplifies the formation of the keyhole 16.

The indicated condition for the formation of a keyhole can also occur where a high aspect ratio through-hole is formed by RIE and where the formation position of the through-hole may deviate from the correct position due to mask misalignment or a process variation. The created through-hole can in this case exhibit a profile that inhibits complete and uniform deposition of HDP-oxide.

The indicated existence of keyholes is, from a semiconductor manufacturing point of view, highly undesirable. Keyhole formation can be the cause of shorts between conducting layers, high leakage currents and unsatisfactory planarization characteristics. What is needed therefore is a method that eliminates the formation of keyholes. This method can solve the problem of keyhole formation by improving the filling of the holes or by reducing the aspect ratio of the hole or by improving the reentrant spacer profile. The present invention addresses the elimination of the keyhole by applying all three indicated problem solutions.

US 5,814,564 (Yao) shows an etch back method to planarize an interlayer having a critical HDP-CVD deposition process.

US 5,756,396 (Lee et al.) teaches full spacers on metal line sidewalls.

US 5,262,352 (Woo) Method for forming an interconnection structure for conductive layers - shows a method for forming spacers on metal line sidewalls.

US 5,462,893 (Matsuoka et al.) shows a spacer used as an etch stop on a metal line.

SUMMARY OF THE INVENTION

It is the primary objective of the invention to eliminate the formation of intra-space irregularities or keyholes within the Intra-Layer Dielectric of a pattern of conducting lines.

It is a further objective of the present invention to reduce leakage current within the pattern of conducting lines.

It is a further objective of the invention to enhance inter-layer planarity within a semiconductor structure.

It is a further objective of the invention to reduce the aspect ratio of holes within a semiconductor structure.

It is a further objective of the invention is to improve the spacer profile of reentrant spacers within holes.

It is a further objective of the invention to reduce circuit failure and conduction layer shorts within a semiconductor structure.

In accordance with the objectives of the invention, a new method of depositing PE-oxide or PE-TEOS is achieved for use

as an ILD within a conducting line pattern. An HDP-oxide is deposited over a pattern of polysilicon. A Buffered Oxide Etch (BOE) dip-back is performed on the surface of the deposited HDP-oxide leaving a layer of HDP-oxide on the bottom of the holes between the conducting lines in addition to leaving HDP-oxide on the top surface of the pattern of conducting lines. A layer of plasma-enhanced SiN is deposited. This PE-SiN is etched back leaving SiN spacers on the sidewalls of the poly pattern. The profile of the holes within the poly pattern is now such that the final layer of PE-oxide or PE-TEOS can be deposited without resulting in the formation of keyholes.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section of a Prior Art deposition of a layer of HDP-oxide and the formation of keyholes within a poly pattern.

Fig. 2 shows a cross section of a Prior Art deposition of a layer of HDP-oxide and the formation of keyholes within a poly pattern whereby the poly pattern has spacers on the sidewalls of the pattern.

Fig. 3 shows a cross section of a polysilicon pattern.

Fig. 4 shows a cross section of a polysilicon pattern over which a layer of HDP-oxide has been deposited.

Fig. 5 shows a cross section after a Buffered Oxide Etch (BOE) dip back has been performed on the deposited layer of HDP-oxide.

Fig. 6 shows a cross section of the polysilicon layer after a layer of SiN has been deposited over the etched back HDP-oxide.

Fig. 7 shows a cross-section after SiN etch back of the deposited layer of SiN.

Fig. 8 shows a cross section of the polysilicon pattern after the deposition of the final layer of PE-oxide or PE-TEOS.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now specifically to Fig. 3, there is shown a pattern of polysilicon 20 deposited on top of a surface 15.

The opening 22 is assumed to have an aspect ratio that is larger than 3.

The deposited poly 20 typically has a height of between 2 and 6K Angstrom, the width of pattern 22 typically is 0.2 um with a spacing between pattern openings of 0.3 um.

Fig. 4 shows the deposition of a layer 40 of HDP-oxide over the pattern 20 of polysilicon. It is to be noted that the surface of the HDP-oxide layer 40 is not planarized at this time and is highly contoured by the profile of the underlying pattern 20 of polysilicon. This aspect of the invention is important since by maintaining the profile as shown the subsequent steps can form the desired spacers (which in turn prevent the formation of keyholes) and reduce the aspect ratio of the hole. For the non-SAC process, layer 20 contains only polysilicon, for the SAC process layer 20 contains a lower layer of polysilicon and a top layer (about 2000 Angstrom thick) of SiN. The HPD-oxide is deposited using HTP and LPCVD technology, to a thickness of between about 2 and 6K Angstrom.

Fig. 5 shows the results of a Buffered Oxide Etch dip-back. Of importance in this dip-back is the profile and amount 54 of the HDP-oxide that remains in place after this dip-back.

The height of layer 54 of HDP-oxide is directly instrumental in reducing the aspect ratio of the hole between the poly pattern 20 because this layer 54 of HDP-oxide raises the bottom of the hole. The profile of the remaining HDP-oxide highlighted as 52 is instrumental in reducing the formation of the keyhole because this HDP-oxide enables or facilitates the penetration of the later to be deposited HDP-oxide into the hole. This HDP-oxide (52) urges the final layer of deposited PE-oxide or PE-TEOS into the hole and, in doing so, prevents the formation of the keyhole. The typical average thickness of layer 54 after completion of the etch back is about 4 K Angstrom. Layer 52 has a typical height of between 4 and 5 K Angstrom.

Fig. 6 shows a cross section of the deposition of a layer 60 of SiN. This layer 60 of SiN forms the basis for the formation of the spacers on the sidewalls of the polysilicon pattern 20. The deposition of layer 60 uses PECVD technology, the layer is deposited at a temperature of about 400 degrees C. to a thickness between about 1000 and 2000 Angstrom.

Fig. 7 shows a cross section of the poly pattern after the deposited layer (layer 60, Fig. 6) of SiN has been etched. This etching in effect forms the spacers 70 on the sidewalls

of the poly pattern 20. These spacers 70 will further act to prevent the formation of the keyholes by virtue of their profile and by virtue of their presence. The profile of spacers 70 is such that the profile is curved facing away from the widewalls of the poly pattern. This curvature pushes the to be deposited HDP-oxide toward the center of the hole thus urging the deposition and formation of the HDP-oxide in this center. The HDP-oxide 52 that is on the top surface of the poly pattern performs the same function but performs this function at an earlier stage within the deposition process. Deposition 52 urges the deposited HDP-oxide towards the hole; spacers 70 pack the HDP-oxide inside the hole densely enough and at a rate such that no keyhole formation takes place.

The SiN layer typically is etched using CHF_3 at a flow rate of 15 sccm, with a gas pressure of 50 mTorr, an rf power density of 700 Watts, with no magnetic field applied, and an ambient wafer temperature of about 15 degrees C. End-point for the etch is an CO/CN end point signal.

Fig. 8 shows the deposition of the final layer 80 of PE-TEOS or PE-oxide. Due to the formed spacers 70 and the formation of the previous depositions 52 of HDP-oxide, no

keyholes will be formed. Layer 80 is typically deposited to a thickness of about 1 um.

While the present invention has been shown and described with reference to the preferred embodiment thereof, it will be understood by those skilled in the art of semiconductor manufacturing that the foregoing and other changes may be made therein without departing from the spirit and scope of the present invention.

What is claimed is:

1. A method of filling gaps in the plane of and between the pattern of a wiring structure on a semiconductor substrate, comprising the steps of:

Depositing a first layer of dielectric over said wiring structure thereby including the exposed surface of said semiconductor substrate;

Performing an etch back of said first layer of dielectric;

Depositing a second layer of dielectric over said etched back first layer of dielectric;

Etching said second layer of dielectric; and

Depositing a layer of oxide over said etched second layer of dielectric thereby including said exposed portions of said first layer of dielectric.

2. The method of claim 1 wherein said wiring structure contains polysilicon.

3. The method of claim 1 wherein said wiring structure contains a lower layer of polysilicon and a upper layer of silicon nitride (SiN) said wiring structure to be applied during the SAC process.

4. The method of claim 1 wherein said wiring structure contains an electrically conducting material.

5. The method of claim 1 wherein said first layer of dielectric contains High Density Plasma-oxide.

6. The method of claim 1 wherein said etch back of said first layer of dielectric is performing a Buffered Oxide Etch said etch back to be performed on said first layer of dielectric thereby forming a layer of first dielectric on the bottom of the holes within said wiring structure thereby further forming deposits of said first dielectric said deposits partially overlaying the top surfaces of said wiring structure.

7. The method of claim 6 wherein said BOE has a BOE solution of 10:1 or 50:1.

8. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of silicon nitride (Si_3N_4) said deposition covering the surface of said layer of first dielectric on the bottom of said holes within said wiring structure thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said

wiring structure thereby furthermore covering the surface of the partially exposed top corners of said wiring structure.

9. The method of claim 1 wherein said depositing said second layer of dielectric is depositing a layer of Si_3N_4 using PE-CVD technology at a temperature of about 400 degrees C. said layer to be deposited to a thickness between about 1000 and 2000 Angstrom.

10. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of aluminum oxide (Al_3O_3) said deposition covering the surface of said layer of first dielectric on the bottom of said holes within said wiring structure thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said wiring structure thereby furthermore covering the surface of the partially exposed top corners of said wiring structure.

11. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of dielectric material having a high dielectric constant said deposition covering the surface of said layer of first dielectric on the bottom of the holes within said wiring structure thereby further covering the surface of said first dielectric

partially overlaying the top surfaces of said wiring structure thereby furthermore covering surface of the partially exposed top corners of said wiring structure.

12. The method of claim 1 wherein said etching said second layer of dielectric removing said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on the sidewalls of said wiring structure.

13. The method of claim 1 wherein said etching second layer of dielectric is etching Si_3N_4 using CHF_3 as etchant gas at a flow rate of about 15 sccm and a gas pressure of about 50 mTorr with an rf power density of about 700 watts with no magnetic field applied and an ambient wafer temperature of about 15 degrees C.

14.The method of claim 1 wherein said depositing a layer of oxide is depositing a layer of PE-oxide or PE-TEOS (Plasma Enhanced tetraethosiloxane) over said spacers on said sidewalls of said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes within said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the

top surfaces of said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said wiring structure.

15. The method of claim 1 with the additional step of planarizing said deposited layer of PE-oxide or PE-TEOS said planarization to proceed down to the plane of the top surface of said conducting line pattern thereby completing the process of creating a high-aspect ratio pattern of conducting lines said conducting lines being separated with a high dielectric constant Intra-Layer Dielectric.

16. A method of filling gaps in the plane of and between the pattern of a wiring structure on a semiconductor substrate, comprising the steps of:
Depositing a first layer of dielectric over said wiring structure thereby including the exposed surface of said semiconductor substrate;
Performing an etch back of said a first layer of dielectric wherein said etch back is performing a Buffered Oxide Etch thereby forming a layer of first dielectric on the bottom of said holes within said wiring structure thereby further forming deposits of said first dielectric on the top surfaces

of said wiring structure said deposits partially overlaying the top surfaces of said wiring structure;

Depositing a second layer of dielectric said deposition covering said layer of first dielectric on the bottom of said holes within said wiring structure thereby further covering said first dielectric partially overlaying the top surfaces of said wiring structure thereby furthermore covering the partially exposed top corners of said wiring structure;

Etching said second layer of dielectric to remove said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on the sidewalls of said wiring structure;

Depositing a layer of PE-oxide or PE-TEOS over said spacers on the sidewalls of said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes within said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the top surfaces of said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said wiring structure.

17. The method of claim 16 wherein said wiring structure contains polysilicon.

18. The method of claim 16 wherein said wiring structure contains a lower layer of polysilicon and a upper layer of silicon nitride (SiN) said wiring structure to be applied during the SAC process.

19. The method of claim 16 wherein said wiring structure contains an electrically conducting material.

20. The method of claim 16 wherein said first layer of dielectric contains High Density Plasma-oxide.

21. The method of claim 16 wherein said etch back of said first layer of dielectric is a Buffered Oxide Etch (BOE) with a BOE solution of 10:1 or 50:1.

22. The method of claim 16 wherein said depositing said second layer of dielectric is depositing a layer of Si_3N_4 using PE-CVD technology at a temperature of about 440 degrees C. said layer to be deposited to a thickens between about 1000 and 2000 Angstrom.

23. The method of claim 16 wherein said depositing a second layer of dielectric is depositing a layer of aluminum oxide (Al_3O_3).

24. The method of claim 16 wherein said depositing a second layer of dielectric is depositing a layer of dielectric material having a high dielectric constant.

25. The method of claim 16 wherein said etching second layer of dielectric is etching Si_3N_4 using CHF_3 as etchant gas at a flow rate of about 15 sccm and a gas pressure of about 50 mTorr with an rf power density of about 700 watts with no magnetic field applied and an ambient wafer temperature of about 15 degrees C.

26. The method of claim 16 with the additional step of planarizing said deposited layer of PE-oxide or PE-TEOS said planarization to proceed down to the plane of the top surface of said conducting line pattern thereby completing the process of creating a high-aspect ratio pattern of conducting lines said conducting lines being separated with a high dielectric constant Intra-Layer Dielectric.

ABSTRACT

A new method of depositing PE-oxide or PE-TEOS. An HDP-oxide is provided over a pattern of polysilicon. An etch back is performed to the deposited HDP-oxide, a layer of plasma-enhanced SiN is deposited. This PE-SiN is etched back leaving SiN spacers on the sidewalls of the poly pattern, further leaving a deposition of HDP-oxide on the top surface of the poly pattern. The profile of the holes within the poly pattern in such that the final layer of PE-oxide or PE-TEOS is deposited without resulting in the formation of keyholes in this latter layer.

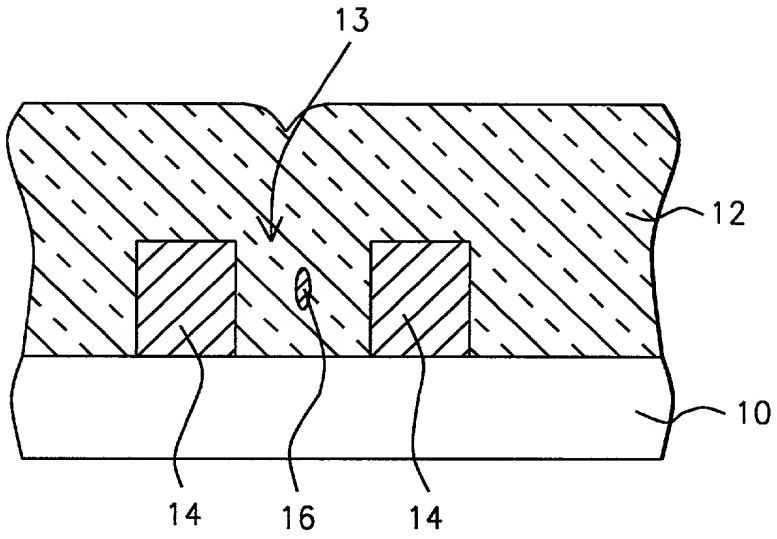

FIG. 1 – Prior Art

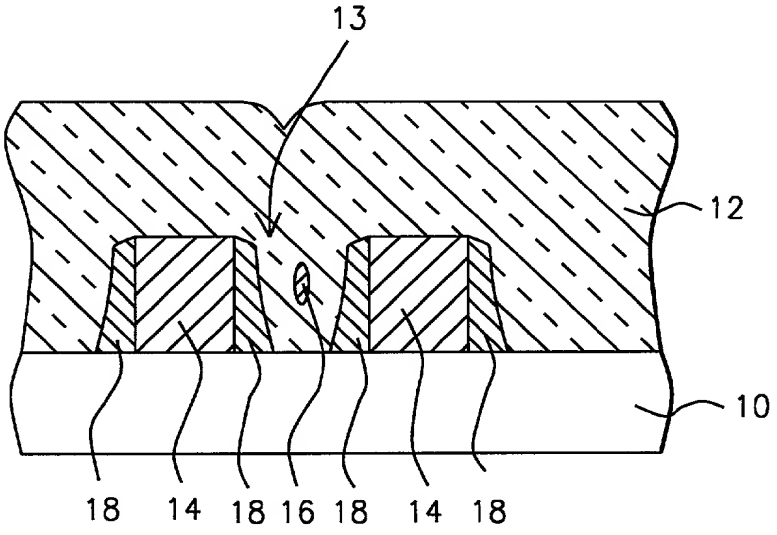

FIG. 2 – Prior Art

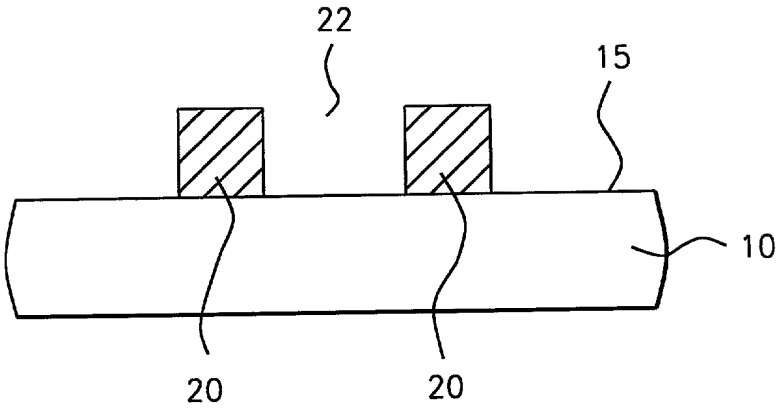

FIG. 3

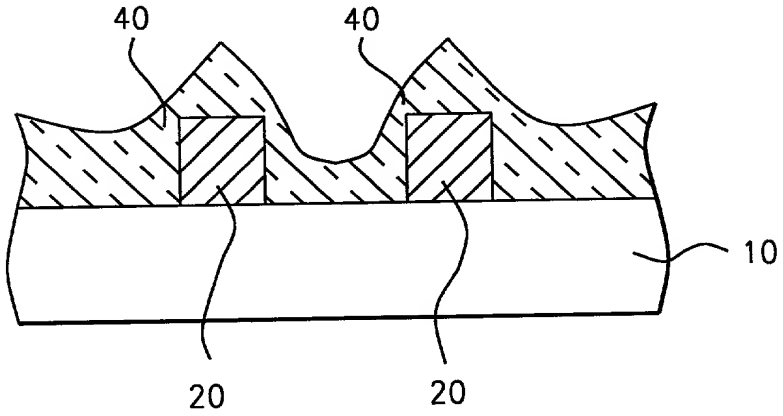

FIG. 4

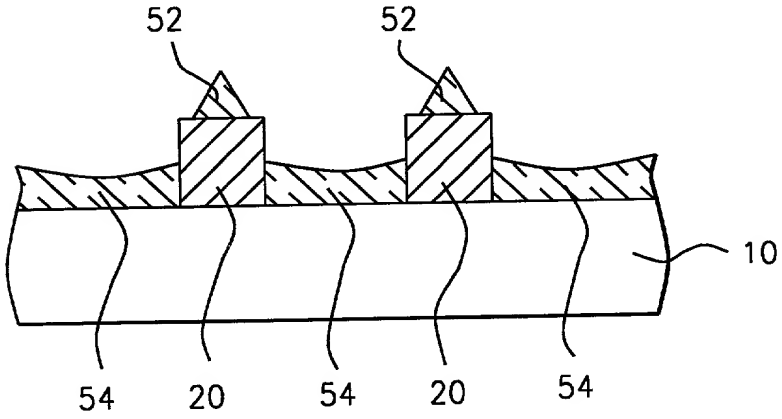

FIG. 5

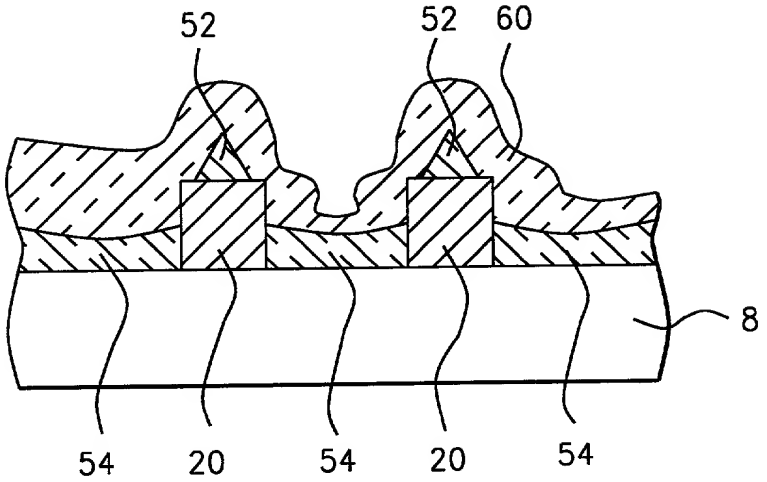

FIG. 6

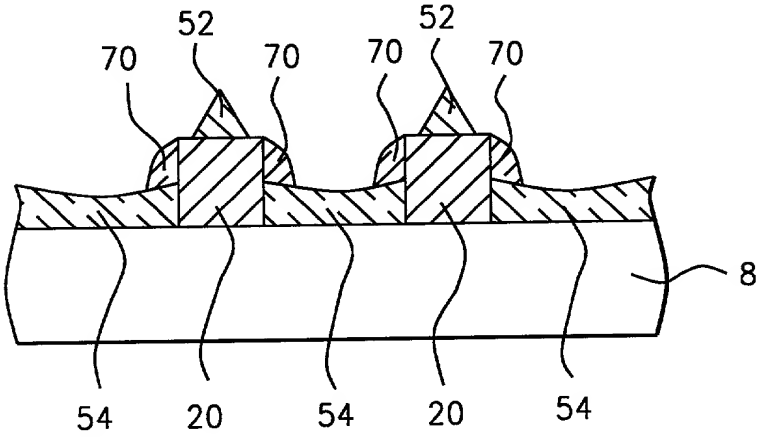

FIG. 7

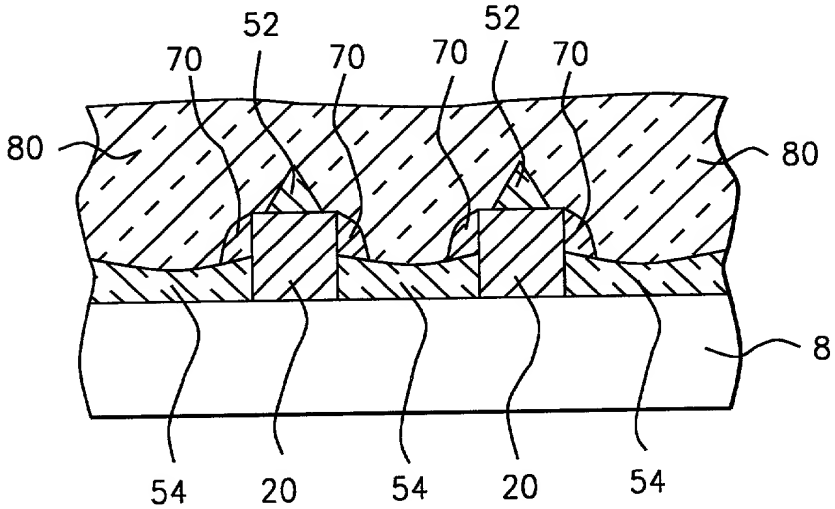

FIG. 8

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

DOCKET NO. **TS98-518**

As a below named Inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **A Key-Hole Free Process For High Aspect Ratio Gap Filling With Reentrant Spacer**

the specification of which (check one)

X is attached hereto.

was filed on _____

Application Serial No. _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above Identified specification including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed:

(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name & registration no.)

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Full name of **sole or first** inventor

Date

Tze-Liang Ying
Inventor's signature

1/6/1999

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DOCKET NO. **TS98-518**

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Full name of **second** inventor (Last name first) Date

James Wu 1/6/1999
Inventor's signature

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YU-HUA LEE
Full name of **third** inventor Date

Yu Hua Lee 1/6/1999
Inventor's signature

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Republic of China, Taiwan
Citizenship

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Post Office Address

Full name of **fifth** inventor Date

Inventor's signature

Residence

Citizenship

Post Office Address

Full name of **sixth** inventor Date

Inventor's signature

Residence

Citizenship

Post Office Address